

# 16 Volt Digitally Programmable Potentiometer (DPP™) with 128 Taps and an Increment Decrement Interface



#### **FEATURES**

- Single linear DPP with 128 taps
- End-to-end resistance of 10kΩ, 50kΩ or 100kΩ
- 2-wire interface
- Fast Up/Down wiper control mode
- Non-volatile wiper setting storage
- Automatic wiper setting recall at power-up
- Digital Supply range (V<sub>cc</sub>): 2.7V to 5.5V
- Analog Supply range (V+): +8V to +16V
- Low Standby Current: 15µA
- 100 Year wiper setting memory
- Industrial Temperature range: -40°C to +85°C
- RoHS-compliant 10-pin MSOP package

#### APPLICATION

- LCD screen Adjustment
- Volume Control
- Mechanical potentiometer replacement
- Gain adjustment
- Line impedance matching
- VCOM settings adjustment

For Ordering Information details, see page 9.

#### **BLOCK DIAGRAM**

#### **VCC** UP/DOWN (U/<del>D</del>) ◀ 127 $R_{H}$ CONTROL LOGIC AND (INC) ADDRESS DECODE Device Select RESISTIVE 128 TAP POSITION DECODE CONTROL 7-BIT 7-BIT WIPER NONVOLATILE CONTROL MEMORY REGISTER REGISTER (WCR) (DR)

#### DESCRIPTION

The CAT5133 is a high voltage Digital Programmable Potentiometer (DPP) integrated with EEPROM memory and control logic to operate in a similar manner to a mechanical potentiometer. The DPP consists of a series of resistive elements connected between two externally accessible end points. The tap points between each resistive element are connected to the wiper outputs with CMOS switches. A 7-bit wiper control register (WCR) independently controls the wiper tap switches for the DPP. Associated with the control register is a 7-bit nonvolatile memory data register (DR) used for storing the wiper settings. Changing the value of the wiper control register or storing that value into the nonvolatile memory is performed via a 3-input Increment-Decrement interface.

The CAT5133 comes with 2 voltage supply inputs:  $V_{\rm CC}$  (digital supply voltage) input and V+ (analog bias supply) input. Providing separate Digital and Analog inputs allow the potentiometer terminals to be as much as 10 volts above  $V_{\rm CC}$  and 16 volts above ground.

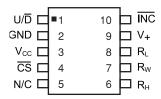
The CAT5133 can be used as a potentiometer or as a two terminal, variable resistor. It is designed for circuit level or system level adjustments in a wide variety of applications.

On power-up, the contents of the nonvolatile data register (DR) are transferred to the wiper control register (WCR) and the wiper is positioned to that location. The CAT5133 is shipped with the DR programmed to position 64.



## PIN CONFIGURATION

## MSOP Package (GZ)



## **PIN DESCRIPTIONS**

Pin	Name	Function
1	U/D	Up/Down Data Input – Determines the direction of movement of the wiper
2	GND	Ground
3	$V_{CC}$	Logic Supply Voltage (2.7V to 5.5V)
4	CS	Chip Select – The chip is selected when the input is low.
5	N/C	No Connect
6	R <sub>H</sub>	High Reference Terminal for the Potentiometer
7	$R_W$	Wiper Terminal for the Potentiometer
8	$R_L$	Low Reference Terminal for the Potentiometer
9	V <sub>+</sub>	Analog Bias Voltage Input (+8.0V to +16.0V)
10	ĪNC	Increment Input – Moves the wiper in the direction determined by the Up/Down input on each negative edge

## **DEVICE OPERATION**

The CAT5133 operates like a digitally controlled potentiometer with  $R_{\text{H}}$  and  $R_{\text{L}}$  equivalent to the high and low terminals and  $R_{\text{W}}$  equivalent to the mechanical potentiometer's wiper. There are 128 available tap positions including the resistor end points,  $R_{\text{H}}$  and  $R_{\text{L}}$ . There are 127 resistor elements connected in series between the  $R_{\text{H}}$  and  $R_{\text{L}}$  terminals. The wiper terminal is connected to one of the 128 taps and controlled by three inputs,  $\overline{\text{INC}}$ , U/\overline{D} and  $\overline{\text{CS}}$ . These inputs control a 7-bit up/down counter whose output is decoded to select the wiper position. The selected wiper position can be stored in nonvolatile memory using the  $\overline{\text{INC}}$  and  $\overline{\text{CS}}$  inputs.

With  $\overline{\text{CS}}$  set LOW the CAT5133 is selected and will respond to the U/ $\overline{\text{D}}$  and  $\overline{\text{INC}}$  inputs. HIGH to LOW transitions on  $\overline{\text{INC}}$  will increment or decrement the

wiper (depending on the state of the U/ $\overline{D}$  input and 7-bit counter). The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. The value of the counter is stored in nonvolatile memory whenever  $\overline{CS}$  transitions HIGH while the  $\overline{INC}$  input is also HIGH. When the CAT5133 is powered-down; the last stored wiper counter position is maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is set to the value stored.

With INC set low, the CAT5133 may be de-selected and powered down without storing the current wiper position in nonvolatile memory. This allows the system to always power up to a preset value stored in nonvolatile memory.

#### **OPERATION MODES**

ĪNC	CS	U/D	Operation
High to Low	Low High Wip		Wiper toward H
High to Low	Low	Low	Wiper toward L
High	Low to High X		Store Wiper Position
Low	Low to High	Х	No Store, Return to Standby
X	High	High X Standby	

$$C_{H} \stackrel{R_{H}}{=} R_{W} \qquad R_{W}$$

$$C_{L} \stackrel{R_{L}}{=} R_{L} \qquad \text{Potentiometer}$$

$$Equivalent Circuit$$



#### POWER-ON AND POTENTIOMETER CHARACTERISTICS

The CAT5133 is a 128-position, digital controlled potentiometer. When applying power to the CAT5133,  $V_{\rm CC}$  must be supplied prior to or simultaneously with V+. At the same time, the signals on  $R_{\rm H},\ R_{\rm W}$  and  $R_{\rm L}$  terminals should not exceed V+. If V+ is applied before  $V_{\rm CC},$  the electronic switches of the DPP are powered in the absence of the switch control signals, that could result in multiple switches being turned on. This causes unexpected wiper settings and possible current overload of the potentiometer.

When  $V_{\rm CC}$  is applied, the device turns on at the midpoint wiper location (64) until the wiper register can be loaded with the nonvolatile memory location previously stored in the device. After the nonvolatile memory data is loaded into the wiper register the wiper location will change to the previously stored wiper position.

At power-down, it is recommended to turn-off first the signals on  $R_{\text{H}}$ ,  $R_{\text{W}}$  and  $R_{\text{L}}$ , followed by V+ and, after that,  $V_{\text{CC}}$ , in order to avoid unexpected transitions of the wiper and uncontrolled current overload of the potentiometer.

The end-to-end nominal resistance of the potentiometer has 128 contact points linearly distributed across the total resistor. Each of these contact points is addressed by the 7 bit wiper register which is decoded to select one of these 128 contact points.

Each contact point generates a linear resistive value between the 0 position and the 127 position. These values can be determined by dividing the end-to-end value of the potentiometer by 127. The  $10k\Omega$  potentiometer has a resistance of  $\sim\!79\Omega$  between each wiper position. However in addition to the  $\sim\!79\Omega$  for each resistive segment of the potentiometer, a wiper resistance offset must be considered. Table 8 shows the effect of this value and how it would appear on the wiper terminal.

This offset will appear in each of the CAT5133 end-to-end resistance values in the same way as the  $10k\Omega$  example. However resistance between each wiper position for the  $50k\Omega$  version will be  $\sim 395\Omega$  and for the  $100k\Omega$  version will be  $\sim 790\Omega$ .

#### Potentiometer Resistance and Wiper Resistance Offset Effects

Position	Typical R <sub>w</sub> to R <sub>L</sub> Resistanc for 10kΩ DPP			
0	70Ω or	0Ω + 70Ω		
01	149Ω or	79Ω + 70Ω		
63	5,047Ω or	$4,977\Omega + 70\Omega$		
127	10,070Ω or	$10,000\Omega + 70\Omega$		

Position	Typical R <sub>w</sub> to R <sub>H</sub> Resistan for 10kΩ DPP			
00	10,070Ω or	$10,000\Omega + 70\Omega$		
64	5,047Ω or	$4,977\Omega + 70\Omega$		
126	149Ω or	79Ω + 70Ω		
127	70Ω or	0Ω + 70Ω		

# ABSOLUTE MAXIMUM RATINGS(1)

Parameters	Ratings	Units
Temperature Under Bias	-55 to +125	°C
Storage Temperature	-65 to +150	°C
Voltage on any U/D, INC,& CS Pins with Respect to V <sub>CC</sub> <sup>(2)</sup>	-0.3 to +V <sub>CC</sub> +0.3	V
Voltage on R <sub>H</sub> , R <sub>L</sub> , & R <sub>W</sub> Pins with Respect to V <sub>CC</sub>	V+	V
V <sub>CC</sub> with Respect to Ground	-0.3 to +6.0	V
V+ with respect to Ground	-0.3 to +16.5	V
Wiper Current	±6	mA
Lead Soldering temperature (10 seconds)	+300	°C

#### Notes:

- (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.
- (2) Latch-up protection is provided for stresses up to 100mA on the digital from -0.3V to  $V_{CC}$  +0.3V.



# RECOMMENDED OPERATING CONDITIONS

 $V_{CC}$  = +2.7V to +5.5V

V+ = +8.0V to +16.0V

Operating Temperature Range: -40°C to +85°C

## POTENTIOMETER CHARACTERISTICS

(Over recommended operating conditions unless otherwise stated.)

				Limits		
Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
R <sub>POT</sub>	Potentiometer Resistance (10kΩ)			10		kΩ
R <sub>POT</sub>	Potentiometer Resistance $(50k\Omega)^{(7)}$			50		kΩ
R <sub>POT</sub>	Potentiometer Resistance (100kΩ) <sup>(7)</sup>			100		kΩ
R <sub>TOL</sub>	Potentiometer Resistance Tolerance				±20	%
	Power Rating	25°C			50	mW
I <sub>W</sub>	Wiper Current				±3	mA
R <sub>W</sub>	Wiper Resistance	I <sub>W</sub> = +1mA @ V+ = 12V		70	150	Ω
		I <sub>W</sub> = +1mA @ V+ = 8V		110	200	Ω
$V_{TERM}$	Voltage on R <sub>W</sub> , R <sub>H</sub> or R <sub>L</sub>	GND = 0V; V+ = 8V to 16V	GND		V+	V
RES	Resolution			0.78		%
A <sub>LIN</sub>	Absolute Linearity <sup>(2)</sup>	$V_{W(n)(actual)} - V_{W(n)(expected)}$ (5), (6)			±1	LSB <sup>(4)</sup>
R <sub>LIN</sub>	Relative Linearity <sup>(3)</sup>	V <sub>W(n+1)</sub> - [V <sub>W(n)</sub> +LSB] <sup>(5), (6)</sup>			±0.5	LSB <sup>(4)</sup>
TC <sub>RPOT</sub>	Temperature Coefficient of R <sub>POT</sub>	(1)		±300		ppm/°C
TC <sub>Ratio</sub>	Ratiometric Temperature Coefficient	(1)			30	ppm/°C
C <sub>H</sub> /C <sub>L</sub> /C	Potentiometer Capacitances	(1)		10/10/25		pF
fc	Frequency Response	$R_{POT} = 50k\Omega$		0.4		MHz

#### Notes:

- (1) This parameter is tested initially and after a design or process change that affects the parameter.
- (2) Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
- (3) Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer.

4

- (4)  $LSB = (R_{HM} R_{LM})/127$ ; where  $R_{HM}$  and  $R_{LM}$  are the highest and lowest measured values on the wiper terminal.
- (5) n = 1, 2, ..., 127.
- (6)  $V^{\dagger}$  @  $R_H$ ; 0V @  $R_L$ ;  $V_W$  measured @  $R_W$ , with no load.
- (7) Contact factory for availability on this version of the CAT5133.



# DC ELECTRICAL CHARACTERISTICS

 $V_{CC}$  = +2.7V to +6.0V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Max	Units
I <sub>CC1</sub>	Power Supply Current	$V_{CC}$ = 5.5V, $f_{INC}$ = 1MHz, Input = GND		1	mA
I <sub>CC2</sub>	Power supply Current Nonvolatile WRITE	$V_{CC}$ = 5.5V, $f_{INC}$ = 1MHz, Input = GND		3.0	mA
I <sub>SB(VCC)</sub>	Standby Current (V <sub>CC</sub> = 5V)	V <sub>IN</sub> = GND or V <sub>CC</sub> , INC = VCC		5	μΑ
I <sub>SB(V+)</sub>	V+ Standby Current	V <sub>CC</sub> = 5V, V+ = 16V		10	μΑ
I <sub>LI</sub>	Input Leakage Current	$V_{IN}$ = GND to $V_{CC}$		10	μΑ
I <sub>LO</sub>	Output Leakage Current	$V_{OUT}$ = GND to $V_{CC}$		10	μΑ
V <sub>IL</sub>	Input Low Voltage		-1	V <sub>CC</sub> x 0.3	V
V <sub>IH</sub>	Input High Voltage		V <sub>CC</sub> x 0.7	V <sub>CC</sub> + 1.0	V
V <sub>OL1</sub>	Output Low Voltage (V <sub>CC</sub> = 3.0V)	I <sub>OL</sub> = 3 mA		0.4	V

## **CAPACITANCE**

 $T_A = 25^{\circ}C$ , f = 1.0MHz,  $V_{CC} = 5.0V$ 

Symbol	Parameter	Test Conditions	Min	Max	Units
C <sub>I/O</sub>	Input/Output Capacitance (SDA)	$V_{I/O} = 0V^{(1)}$		8	pF
C <sub>IN</sub>	Input Capacitance (A0, A1, SCL)	$V_{IN} = 0V^{(1)}$		6	pF

# POWER UP TIMING(1)(2)

Symbol	Parameter	Min	Max	Units
t <sub>PUR</sub>	Power-up to Read Operation		1	ms
t <sub>PUW</sub>	Power-up to Write Operation		1	ms

## **WIPER TIMING**

Symbol	Parameter	Min	Max	Units
t <sub>WRPO</sub>	Wiper Response Time After Power Supply Stable	5	10	μs
t <sub>WRL</sub>	Wiper Response Time After Instruction Issued	5	10	μs

## WRITE CYCLE LIMITS

Ī	Symbol	Parameter	Min	Max	Units
ſ	t <sub>WR</sub>	Write Cycle Time		5	ms

## **RELIABILITY CHARACTERISTICS**

(Over recommended operating conditions unless otherwise stated.)

Symbol	Parameter	Reference Test Method	Min	Max	Units	
$N_{END}^{(1)}$	Endurance	MIL-STD-883, Test Method 1033	100,000		Cycles/Byte	
T <sub>DR</sub> <sup>(1)</sup>	Data Retention	MIL-STD-883, Test Method 1008	100		Years	

## Notes:

- (1) This parameter is tested initially and after a design or process change that affects the parameter.
- (2) t<sub>PUR</sub> and t<sub>PUW</sub> are the delays required from the time V<sub>CC</sub> is stable until the specified operation can be initiated.

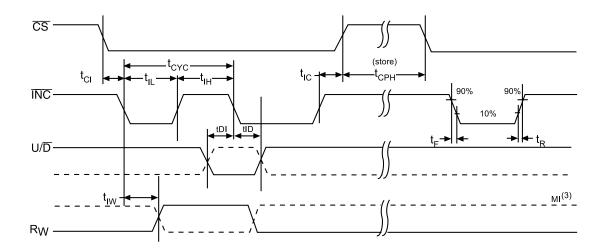


# **A.C. OPERATIONG CHARACTERISTICS**

 $V_{CC}$  = +2.5V to +6.0V,  $V_{H}$  =  $V_{CC}$ ,  $V_{L}$  = 0V, unless otherwise specified.

Symbol	Parameter	Min	Typ <sup>(1)</sup>	Max	Units
t <sub>CI</sub>	CS to INC Setup	100			ns
$t_{DI}$	U/D to INC Setup	50			ns
$t_{ID}$	U/D to INC Hold	100			ns
t <sub>IL</sub>	INC LOW Period	250			ns
t <sub>IH</sub>	INC HIGH Period	250			ns
t <sub>IC</sub>	INC Inactive to CS Inactive	1			μs
t <sub>CPH</sub>	CS Deselect Time (NO STORE)	100			ns
t <sub>CPH</sub>	CS Deselect Time (STORE)	10			ms
t <sub>IW</sub>	INC to VOUT Change		1	5	μs
t <sub>CYC</sub>	INC Cycle Time	1			μs
$t_R, t_F^{(2)}$	INC Input Rise and Fall Time			500	μs
$t_{PU}^{(2)}$	Power-up to Wiper Stable			1	ms
t <sub>WR</sub>	Store Cycle		5	10	ms

# A.C. TIMING



## Notes:

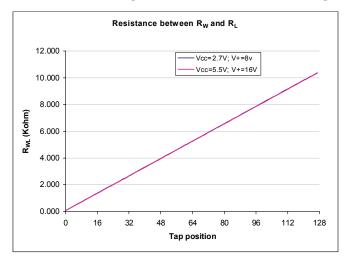
Doc. No. MD-2125 Rev. C

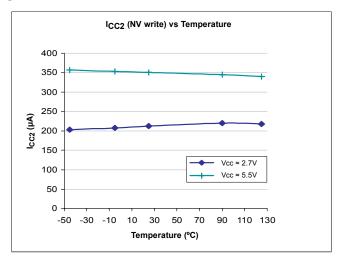
- (1) Typical values are for  $T_A$ =25°C and nominal supply voltage.
- (2) This parameter is periodically sampled and not 100% tested.
- (3) MI in the A.C. Timing diagram refers to the minimum incremental change in the W output due to a change in the wiper position.

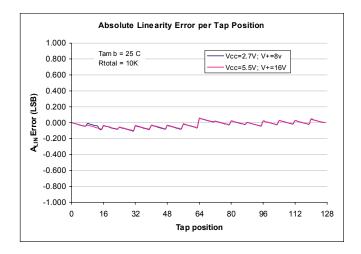
6

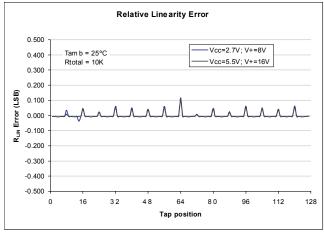


# **TYPICAL PERFORMANCE CHARACTERISTICS**





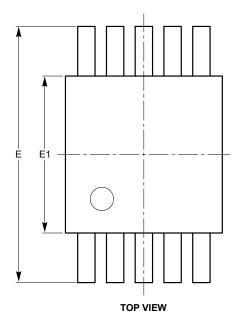




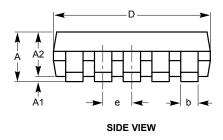


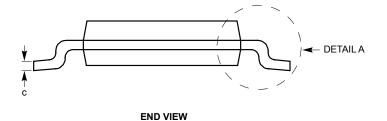
# **PACKAGE OUTLINE DRAWINGS**

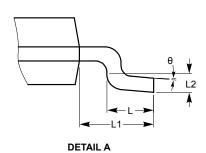
MSOP 10-Lead 3.0 x 3.0mm (Z)  $^{(1)(2)}$ 



SYMBOL	MIN	NOM	MAX
Α			1.10
A1	0.00	0.05	0.15
A2	0.75	0.85	0.95
b	0.17		0.27
С	0.13		0.23
D	2.90	3.00	3.10
Е	4.75	4.90	5.05
E1	2.90	3.00	3.10
е		0.50 BSC	
L	0.40	0.60	0.80
L1	0.95 REF		
L2	0.25 BSC		
θ	0°		8°







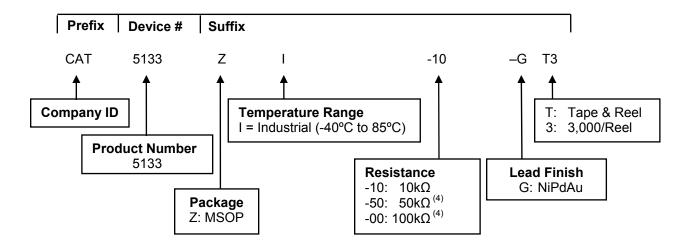
For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

## Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC Specification MO-187.



## **EXAMPLE OF ORDERING INFORMATION**



## **ORDERING PART NUMBER**

CAT5133ZI-10-GT3		
CAT5133ZI-50-GT3 <sup>(4)</sup>		
CAT5133ZI-00-GT3 <sup>(4)</sup>		

For Product Top Mark Codes, click here: http://www.catsemi.com/techsupport/producttopmark.asp

#### Notes

- (1) All packages are RoHS-compliant (Lead-free, Halogen-free).
- (2) The standard lead finish is NiPdAu.
- (3) The device used in the above example is a CAT5133ZI-10-GT3 (MSOP, Industrial Temperature range, 10kΩ, NiPdAu, Tape & Reel, 3 000/Reel)
- (4) For additional package and temperature options, please contact your nearest Catalyst Semiconductor Sales office.

## **REVISION HISTORY**

Date	Rev.	Reason
04/28/06	Α	Initial Issue
11/03/06	В	Update Ordering Information
03/14/2008	С	Update Package Outline Drawing Add MD- to Document Number Add Link to Top Mark Codes

#### Copyrights, Trademarks and Patents

© Catalyst Semiconductor, Inc.

Trademarks and registered trademarks of Catalyst Semiconductor include each of the following:

Adaptive Analog™, Beyond Memory™, DPP™, EZDim™, LDD™, MiniPot™, Quad-Mode™ and Quantum Charge Programmable™

Catalyst Semiconductor has been issued U.S. and foreign patents and has patent applications pending that protect its products.

CATALYST SEMICONDUCTOR MAKES NO WARRANTY, REPRESENTATION OR GUARANTEE, EXPRESS OR IMPLIED, REGARDING THE SUITABILITY OF ITS PRODUCTS FOR ANY PARTICULAR PURPOSE, NOR THAT THE USE OF ITS PRODUCTS WILL NOT INFRINGE ITS INTELLECTUAL PROPERTY RIGHTS OR THE RIGHTS OF THIRD PARTIES WITH RESPECT TO ANY PARTICULAR USE OR APPLICATION AND SPECIFICALLY DISCLAIMS ANY AND ALL LIABILITY ARISING OUT OF ANY SUCH USE OR APPLICATION, INCLUDING BUT NOT LIMITED TO, CONSEQUENTIAL OR INCIDENTAL DAMAGES.

Catalyst Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Catalyst Semiconductor product could create a situation where personal injury or death may occur.

Catalyst Semiconductor reserves the right to make changes to or discontinue any product or service described herein without notice. Products with data sheets labeled "Advance Information" or "Preliminary" and other products described herein may not be in production or offered for sale.

Catalyst Semiconductor advises customers to obtain the current version of the relevant product information before placing orders. Circuit diagrams illustrate typical semiconductor applications and may not be complete.



Catalyst Semiconductor, Inc. Corporate Headquarters 2975 Stender Way Santa Clara, CA 95054 Phone: 408.542.1000

Fax: 408.542.1200 www.catsemi.com

Document No: MD-2125

Revision: C

Issue date: 03/14/08